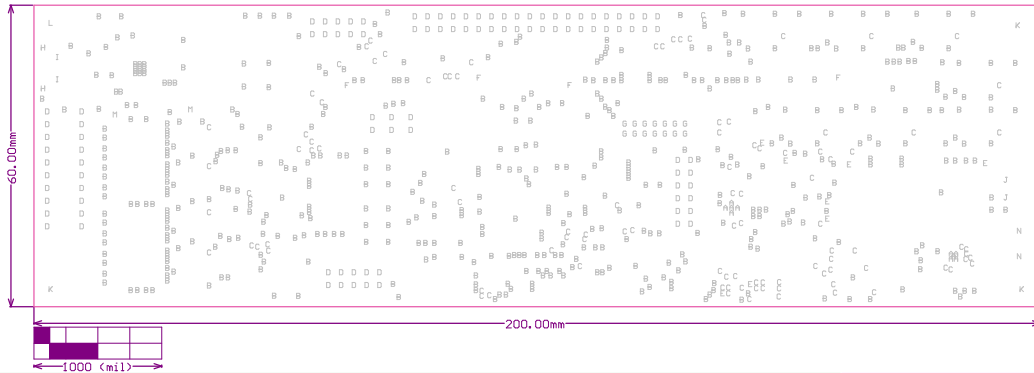


Symbol	Hit Count	Tool Size	Physical Length	Rout Path Length	Plated	Hole Type
A	10	8mil (0.203mm)			PTH	Round
B	104	12mil (0.305mm)			PTH	Round
C	456	16mil (0.406mm)			PTH	Round
D	8	20mil (0.508mm)			PTH	Round
E	2	24mil (0.609mm)			PTH	Round
F	14	32mil (0.813mm)			PTH	Round
G	14	36mil (0.914mm)			PTH	Round
H	98	38mil (0.965mm)			PTH	Round
I	2	40mil (1.016mm)			PTH	Round
J	4	50mil (1.27mm)			NPTH	Round
K	2	52mil (1.321mm)			PTH	Round
L	1	120mil (3.251mm)			PTH	Round
M	9	120mil (3.251mm)			NPTH	Round
N	2	26.55mil (0.659mm)	35.433mil (0.9mm)	9.842mil (0.25mm)	PTH	Slot
O	2	31.455mil (0.8mm)	69.059mil (1.5mm)	27.859mil (0.7mm)	PTH	Slot
748 Total						

Slot definitions : Rout Path Length = Calculated from tool start centre position to tool end centre position.
Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout

Drill Table

DRILL TOLERANCES: FOR PTH +/-2MILS
FOR NPTH +/-2MILS
DRILL TOLERANCES FOR 8 MIL VIA +0/-8mils
DRILL TOLERANCES FOR 12 MIL VIA +0/-12mils
DRILL TOLERANCES FOR 16 MIL VIA +0/-16mils



ALL NETWORK VIEWED FROM TOP SIDE	BOMID #:	TID#-D0171-B	REV:	E3	SUN REV:	Not In VersionControl
LAYER NAME =	Drill Drawing	ISE-ACD-FHB-E3				
PLOT NAME =	Fabrication Drawing	GENERATED :	7/22/2014	2:56:04 PM	TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Layer Stack Up Detail for: ISE-ACD-FHB-E3.PcbDoc

Layer Name	Order	Dielectric	Copper Thickness	Solder Resist
Top Solder Mask	(.615)			Solder Resist
Top Layer	(.015)	1.4mil		
MidLayer1	(.81)	1.4mil		F2-4
MidLayer2	(.82)	1.4mil		F2-4
Bottom Layer	(.085)	1.4mil		F2-4
Bottom Solder Mask	(.085)			Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)

7874MIL X 2352MIL

Number of Layers : 4

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 7.5 MIL

MIN. VIA PAD SIZE: 20 MIL

MINIMUM ANNULAR RING 0.15mm (6MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- .5 MIL; HOLES +/- .3 MIL

IT IS NOT IMPEDANCE CONTROLLED BOARD

VIA'S ARE TENTED

MATERIAL:

☒ FR-408 ☐ FR-4 High Tg ☐ OTHER

THICKNESS: ☒ 63 MIL (1.6mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI PC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

BOW & TWIST: ☒ ANSI PC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

COPPER THICKNESS (FINISHED):

OUTER: ☒ 1.4MIL (1oz) ☐ 2MIL (1.4oz) ☐ 2.8MIL (2oz)

INNER SIGNAL: ☒ 1.4MIL (1oz) ☐ 2.8MIL (2oz) ☐ N/A

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES

PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR:

☒ GREEN ☐ BLUE ☐ OTHER

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENERPIG

☐ MM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL:

☐ CUT AND TRIM PER MECH LAYER 1

☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCB'S TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI PC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3

☒ UL 94V-0 ☒ RoHS ☐ OTHER ☐ PER ORDER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BAKE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

MANUFACTURER'S UL: ☐ RAL ☐ METAL ☒ SILK



PROJECT TITLE:
ISE-ACD-FHB-E3

DESIGNED FOR:
Public Release

FILE NAME:
ISE-ACD-FHB-E3.PcbDoc

ENGINEER:
Navaneeth/Atul

LAYOUT BY:

SCALE: 0.67

ALTM DESIGNER VERSION:
10.0.0.27008